



THE ROPE MEMORY—A PERMANENT STORAGE DEVICE

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INTRODUCTION

A powerful way of increasing the capability and flexibility of digital computing systems is through the use of permanent storage memories. Such memories are also known as read-only memories or NDRO electrically unalterable memories. As an example of the application of a permanent memory, consider a computer used for control purposes. Generally, such systems are physically small, relatively inexpensive, and are not required to perform a variety but rather a restricted category of computations. The problem of program and constant input and storage in such systems is considerable. Permanent memory can satisfy the input and storage function required in such a system in an inexpensive manner. It can, furthermore, be packaged in such a manner as to minimize volume requirements; in any event, the volume occupied by the store for such an application is less than that required for tape or other inputs. In both large and small scale computers, permanent memory can be used for the storage of supervisory routines, input/output function routines, and, in the case of the rope memory, performing logic.

The rope memory is a true permanent storage device in that the information content of the memory is fixed by construction; any changes in the information content require that the device be rebuilt or exchanged. Memories in which data can be altered by replacing a changeable data element are classed as "semi-permanent memories". While this distinction may be

logically tenable, it will not be considered in this paper: the changeability being considered here as simply a special case of rebuilding. Rope memories have been used in a number of computing systems; the use of a rope memory in a computer being designed by the M.I.T. Instrumentation Laboratory for the Apollo space craft was announced recently.¹⁵

The emphasis of this paper is on rope memories. The relation of a rope memory to a conventional read/write memory can only be based on the question of whether or not a permanent storage device can be used in a particular application. In order to place the properties of rope memories in their proper place in the class of permanent storage devices, some other techniques of this type will be discussed. (No comparison will be attempted with permanent memories based on optical or photographic principles.) These other techniques have received more attention up to now; the discussion to follow is based on the belief that ropes merit similar attention, all the more so since they give the opportunity for a greater range of applications.

REVIEW OF SOME PERMANENT MEMORY SCHEMES

Before entering on a discussion of rope memories, we shall briefly describe various other permanent memory schemes, the description of which will help in placing the information concerning rope memories into proper perspective. The permanent memory schemes to be described

below are 1) capacitive type, 2) electromagnetic coupling type, and 3) permanent magnet twistor type. These memories have in common the following features:

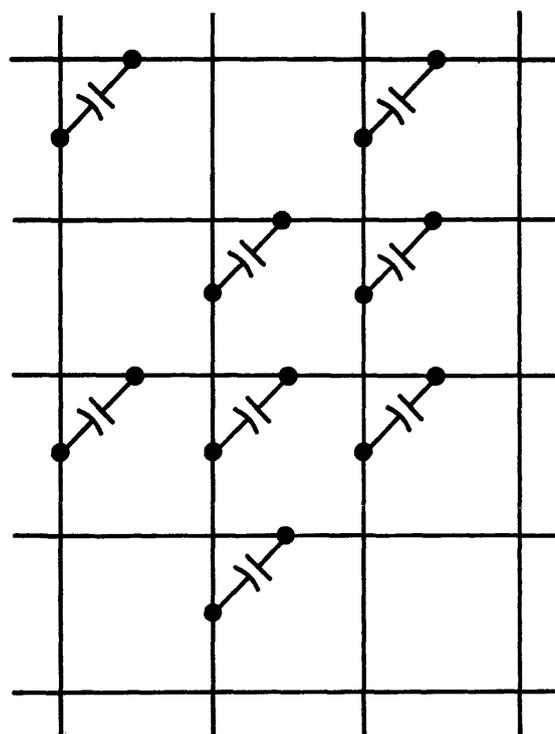
- 1) They are organized in a linear select mode.
- 2) Each storage element stores one bit of information.
- 3) Output signals are of the order of a few millivolts.
- 4) The information state of the memories can be changed by a relatively uncomplicated procedure, i.e., by changing cards which form the basis of information storage.
- 5) Access is random
- 6) Some batch fabrication techniques are possible.

At the conclusion of the discussion concerning rope memories, we shall return to these points and examine them in the light of the behavior of rope memories.

Capacitive Type^{4, 11, 14, 20}

Schematically, this memory can be represented as shown in Figure 1. A voltage pulse directed along any one of the horizontal word lines will be detected on a sense line if that line is coupled to the word line by a capacitor; otherwise, no pulse will appear on the sense line. An interrogation pulse applied to a word line causes all bits of that word to be read out in parallel.

The word and sense lines are etched on separate printed circuit boards. These boards are then oriented in such a manner that the word and sense lines are orthogonal. A metallized card insulated on both sides by a layer of mylar is sandwiched in between these boards. If a hole is punched in the card at the position where a word and sense line intersect, a small (about 1 pf) capacitor is created, thus coupling the sense to the word line corresponding to a "1" bit. The absence of a hole makes capacitive coupling between the lines impossible. Writing is thus accomplished by punching holes in the metallized card in a pattern in accordance with the information to be stored. The metallized card itself is grounded. Memories of this type have been reported to operate at 5 mc rates, with outputs of about 1 mv for storage capacity



**WORD LINES ARE HORIZONTAL
SENSE LINES ARE VERTICAL**

Figure 1. Schematic representation of the capacitive permanent memory.

of 10^5 bits. Worst case analysis of noise conditions shows that a S/N ratio of 10:1 is attainable.

The techniques for fabricating memories of this type are evidently suited to batch processes that should yield relatively inexpensive stores. Mechanical alignment is a problem that must be considered in the design of this type memory. The information state of the memory can be changed by changing the punched metallized cards.

*Electromagnetic Coupling Type*³

This particular technique is based on the fact that the mutual inductance between two conductors having a fixed geometrical relationship is a function of the medium separating them. If an alternating current, I , is caused to flow in one of a pair of one-turn coils, an output will be generated across the terminals of the second coil which is proportional to $M_0 \cdot dI/dt$. The

induced emf in the second coil can be reduced, for a constant geometry, by inserting a shielding material between the coils. Thus, for example, the insertion of a copper plate of 0.04 mm thickness between two coils of 6.5 mm diameter separated by a distance of 0.75 mm causes a 23 db reduction in the induced emf. Binary information can thus be stored as the absence or presence of shield between the coils and can be detected as the absence or presence of an induced emf.

The primary coil is the *excitation* coil; the secondary coil is the *sensing* coil. Since excitation coils and sensing coils can be connected in series as shown in Figure 2, it is possible to manufacture arrays of coils by printed circuit techniques. The excitation coils are etched on one board, the sensing coils are etched on a second board. The orientation of these two boards relative to one another is such that the long axes are orthogonal. Each row of excitation coils represents one word, the sensing coils represent bits. The system is word organized.

Storage of information is effected by sandwiching a prepunched, insulated metal card between a pair of boards containing excitation and sensing coils. Holes are punched at the intersection of sensing and excitation coils at positions which are to store "1" bits. At positions which are to store "0" bits, no holes are punched. The relative outputs have already been discussed above. Mechanical alignment is

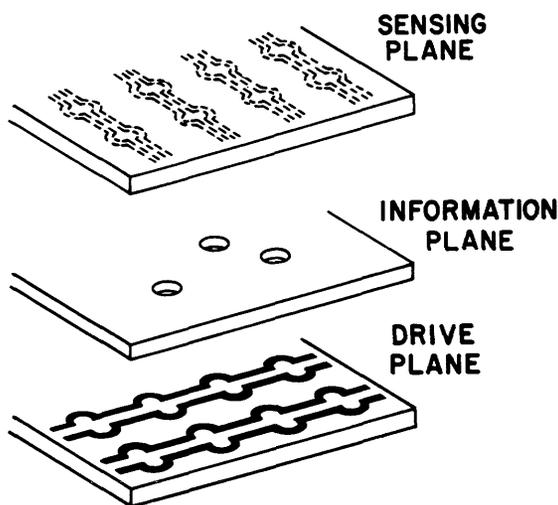


Figure 2. Electromagnetic coupling type permanent memory construction.

extremely critical here, since the holes must have a very definite geometrical relationship to the sense and excitation coils in order not to affect the mutual inductance. Again, stored information can be changed by exchanging cards. A memory of this type is reported as operating at 1.5 mc. Excitation currents used were 200 ma. Outputs are not explicitly reported but can be computed to be about 50 mv without taking attenuation into account. Worst case S/N ratios at the amplifier output are reported to be 30 db.

Permanent Magnet Twistor Type^{2, 5, 7, 10}

The twistor is employed in a novel manner in this type of memory. Information is not stored in the twistor, but rather as the absence or presence of permanent magnets. Associated with each twistor element, there is a permanent magnet whose function is to generate an external field which will inhibit the twistor from switching if that element is to store a "0" bit. Alternately, if the twistor element is to store a "1" bit, it is not to be inhibited from switching, hence no permanent magnet is associated with it. Those twistors inhibited from switching will not change state on being interrogated; those twistors not inhibited will switch from one remanent state to the other upon being interrogated. It is thus necessary to follow up each interrogation pulse with a reset pulse.

In constructing a permanent magnet twistor type memory, the first step is to enclose twistor wires and their returns within mylar tape. This assembly is then bonded to solenoid mounting boards. The solenoids themselves are prepared by photoetching. The permanent magnets are a nickel-cobalt alloy, and are formed on a card either by photoetching or electrodeposition. Some 2,816 permanent magnets (bits) can be deposited on a card having an area of 55 in², giving a density of about 52 bits/in². The twistor wires and tape are continuous; the assembly of wire, tape, and solenoid boards is folded concertina fashion into a stack. Provision is made to guide the magnet card into proper registration with the solenoid board. (It is easy to imagine that alignment problems are critical here, especially in view of the fact that twistor elements may interact if spaced too closely together.) Memories with capacities of

1.44×10^6 bits have been reported, with an operational cycle of $5 \mu\text{sec}$. Drives required are 2.0 amperes for the solenoids. Outputs shown for a 4,096 word module are 4 mv for "ones" and 0.8 mv for "zeroes", with a switching time of about $2 \mu\text{sec}$.

THE ROPE MEMORY^{1, 6, 8, 15, 21}

Principle of Operation

To illustrate the principle of operation of rope memories, suppose that a rope is to be constructed using 2^n cores. It must be possible to select each core uniquely. For purposes of selection, each core is threaded by a selected set of n out of $2n$ inhibit lines. All cores are also threaded by a common set and reset line. Initially all cores are in the same remanent state. Two inhibit registers are used for the purpose of selecting a given core. One of the registers stores the address of the core to be selected, the other register stores the complemented address of the core. These are the D and C registers respectively. Associated with each of the $2n$ bits in the registers is a driver which is enabled if the bit is a "1"; one driver is connected to one inhibit line. The set line is enabled simultaneously with the inhibit lines; the set and inhibit pulses are of equal amplitude but opposite polarity. The amplitude of each pulse is greater than the switching threshold of the core. The polarity of the set pulse is such that in the absence of any inhibit pulses it will switch a core fully. The polarity of the inhibit pulses is such as to prevent a core from switching—the inhibit pulses will drive the core further into saturation.

The selected core is not threaded by any of the enabled inhibit lines and is thus switched by the set pulse. During this phase of the operation (called the selection phase), the cores act as null decoders²¹. Referring to Figure 3, we see that the core will be set if, and only if, none of the threaded \bar{D}_n or \bar{C}_n line drivers is enabled. Hence,

$$\overline{\bar{D}_0 + \bar{C}_1 + \bar{C}_2} = D_0 C_1 C_2 = 1$$

$$\overline{\bar{D}_0 + \dots + \bar{D}_n + \bar{C}_1 + C_2 + \dots} = D_0 \dots D_n \cdot C_1 \cdot C_2 = 1$$

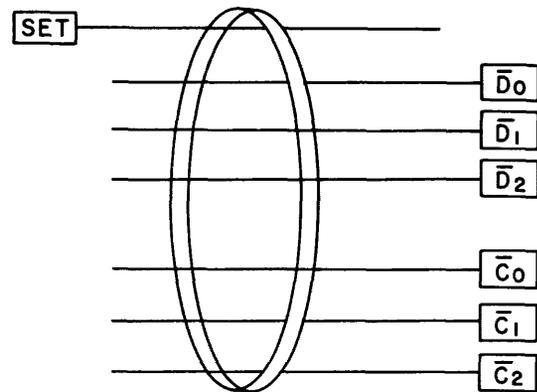


Figure 3.

The reset pulse is of the same amplitude as the set and inhibit pulses. Its polarity is such that it will reset the core that was set during the selection phase of the rope memory operating cycle. During the read phase the core output obtained as a consequence of the application of the reset pulse is used to generate the information pattern. At the end of the reset pulse, all cores are again in the same remanent state. This selection scheme is also known as the Rajhman switch¹⁶.

Each core may store m bits; this requires the use of m sense lines. Information patterns are generated by threading a sense line through a core if the bit to be stored is a "1"; otherwise, the core is bypassed by the particular sense line—these lines correspond to "0" bits as no output will appear across them when the core is reset. The sense lines are common to all cores; a given sense line will thread those cores wherein a "1" is to be stored in the bit position represented by that sense line and will bypass those cores wherein a "0" is to be stored in the bit position represented by that sense line.

Figure 4 illustrates the wiring scheme for a rope memory of eight words ($n=3$). In the illustration each core stores a three-bit word. The information stored is the address of the word storing it. For a rope consisting of eight cores, there are six inhibit lines; three of these are associated with the direct register, the other three lines are associated with the complemented register. Assume that the data stored in word 010 is to be read out. The operation is as follows:

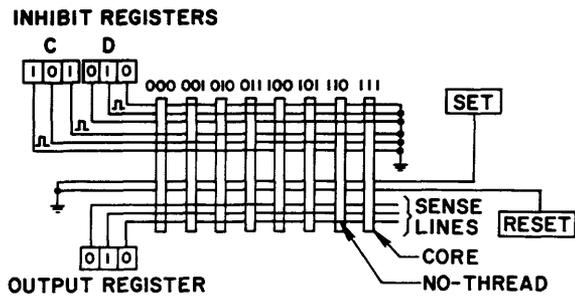


Figure 4a. Rope Memory Wiring Scheme.

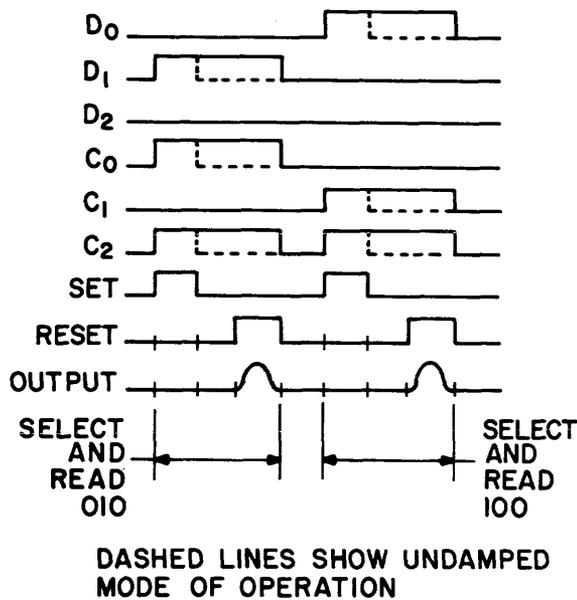


Figure 4b. Timing Diagram for Rope Memory Operation.

- 1) 010 is stored in the direct inhibit register. 101 is stored in the complemented inhibit register.
- 2) During the selection phase, the set line and the drivers corresponding to "1" in the registers are enabled.
- 3) Core 010 will be set since none of the enabled inhibit lines thread it.
- 4) During the read phase, the reset line is enabled and the information stored in the word is transferred to the output register via the sense lines.

The wiring pattern of the inhibit lines can be generalized as shown in Table I. (The LSB of the address is taken as $k=0$.)

TABLE I

k^{th} bit of address	D_k	C_k
0	threads	does not thread
1	does not thread	threads

Rope Organization

Rope memories may be organized in two different ways. The m bits stored by a given core may be considered as the m bits of one word. Alternately, each of the m bits stored by a given rope will be referred to as the "one-core-perferent words. These two ways of organizing a core will be referred to as the "one-core-per-word" and "one-core-per-output bit" modes of storage respectively. Regardless of the organization, the bits stored by any one core are read out in parallel.

A rope organized on a one-core-per-word basis is a random access memory. It is possible to subdivide the m bits stored per core into n equal parts of n bits each so that a core may be considered as storing m/n words of n bits each. This requires that one of m/n sets of sense lines be selected to read out the proper information; for example, if 256 cores are to store four words each for a total of 1024 words, the address must be 10 bits long, eight to select the proper core and two to select the proper one of four words.

A one-core-per-output bit organization requires that the rope be read out sequentially in order that the bits of a word appear in proper order. While this mode of operation is possible, it is not extremely desirable. For one thing, the time elapsed to fully read out a word becomes somewhat prohibitive: given a cycle time of $8\mu\text{sec}$ and a k -bit word, $8k\mu\text{sec}$ would elapse before one word is fully read out. For another thing, the number of bits that a core can store is necessarily related to its inner diameter since this is the factor limiting the number of lines that may be threaded through it. Typically, a core having an I.D. of 0.140" can have 128 sense lines threaded through it. This number of sense lines is certainly adequate for a rope organized on a one-core-per-word basis; it is not necessar-

ily adequate for a rope organized on a one-core-per-output bit basis.

Rope Memory Characteristics

A prototype rope can be seen in Figure 5a. Figure 5b shows a packaged unit. This rope consists of 256 cores, each of which stores four 16-bit words. The storage elements used in this rope are 26 maxwell bobbin cores made of 1/8 mil 4-79 Molybdenum Permalloy. The inner diameter of the bobbins is 0.140". If driven by ramps having a slope of 400 ma/μsec, the output of the rope is of the order of 200 mv, with an absolute S/N of about 9:1. (See Figure 6—Damped Operation.) The switching times of the cores are somewhat less than 2 μsec; but

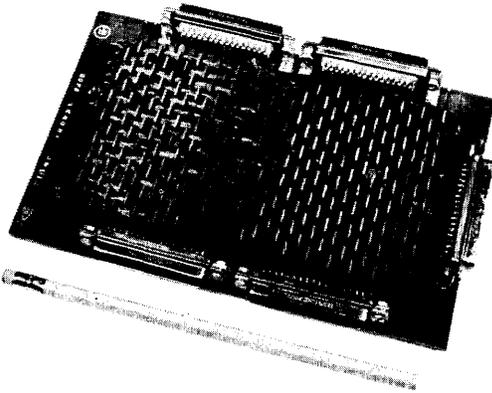
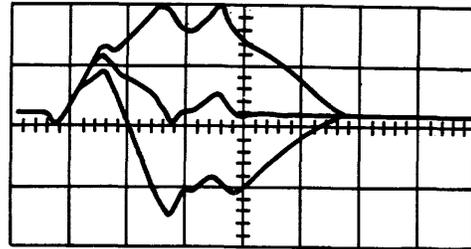


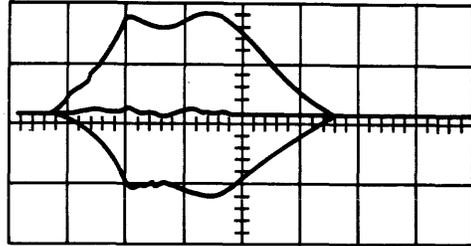
Figure 5a. Prototype Rope Memory Storing 256 Words, 64 Bits per Word.



Figure 5b. Rope Memory Package Capacity: 256 Words, 64 Bits per Word.



UNDAMPED OUTPUT



DAMPED OUTPUT

THE OUTPUTS SHOWN ARE FOR A 256 CORE ROPE OF 64 BITS PER WORD.
BOBBIN CORE: EID #231-002.
SCALES: VERTICAL 100 MV/CM
HORIZONTAL 0.5 USEC/CM

Figure 6. Undamped and damped mode of operation.

since peaking occurs at 2 μsec after the start of the ramp, the cycle time is 8 μsec. The values of resistance and inductance of various lines are tabulated in Table II.

TABLE II

Line	Resistance	Inductance
Set	2 ohms	11 μh
Inhibit	2 ohms	7 μh
Sense	10 ohms	12 μh

These data are suggestive of the performance of a rope memory. Various factors pertaining to rope memory operation are discussed below.

Drive Currents—It is possible to drive ropes with either square pulses or ramps as mentioned above. Owing to the large inductance of the selection and sense lines, a fast rise time pulse makes the $L di/dt$ term large, which introduces 1) considerable back voltage, 2) air coupling noise. While a ramp increases the cycle time of the memory, it 1) introduces rela-

tively little back voltage, 2) decreases air coupling noise, 3) gives greater uniformity of core outputs.

The constraints placed on the various drive currents are relatively minor:

- 1) Each of the set, reset and inhibit pulses must exceed the switching threshold of the core.
- 2) The amplitude of the inhibit pulses must be greater than or equal to the amplitude of the set pulse.
- 3) The set pulse may not start before or end after the inhibit pulses, and must terminate before the reset line is enabled.

There is no requirement that the set and inhibit pulses have the same shape: in fact, it is possible and desirable to apply essentially DC on the inhibit lines; the set pulse may be either a square wave or a ramp, as long as the other constraints are met. The desirability of DC on the inhibit lines will be discussed below in the section on noise cancellation. The reset pulse ought to be a ramp for the reasons advanced above. The relation of the core output to the ramp pulse is shown in Figure 7.

Since the selection scheme associated with rope memories is such that one and only one core is not inhibited from switching during the selection phase and only that core is reset during the read phase, the core may be overdriven in order to increase operating cycles. This will also increase the core output. Clearly, power consumption is increased too.

No general statement can be made regarding the amplitude requirements of the various

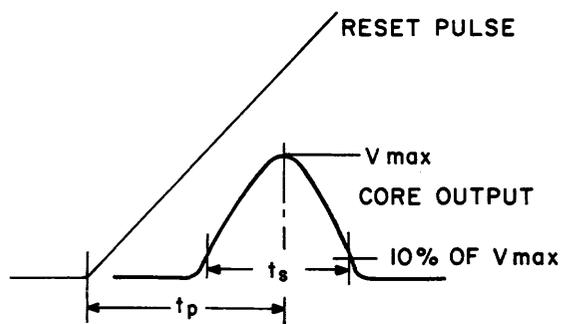


Figure 7. Relation between the core output and the ramp used to generate it.

pulses. As is true in regular coincident current or linear select memories, not all rope memories are made with the same type of core and the magnitude of the threshold switching field is clearly a function of the core used. One vital tradeoff appears in choosing a core for a rope memory: the storage capacity, the required drive currents, and the output voltage are a function of core size. The storage capacity and the required drive currents are directly proportional to the inner diameter of the core; hence, the drive currents increase as the number of bits to be stored increases. It thus becomes axiomatic that for a given required capacity the smallest core making the memory manufacturable is to be selected as the storage element.

Outputs and Noise Cancellation—The output of a particular rope for given drive conditions was given above. This magnitude output is typical for the given slope and memory capacity. The memory capacity governs the output insofar as the length of the sense lines, and hence their attenuation, varies in direct proportion to the number of cores common to a set of sense lines.

Noise problems in rope memories can be rather severe. Fortunately, there are two very simple methods by which noise can be minimized to give S/N ratios of about 10:1. Before discussing these schemes, the causes of the noise in the rope will be discussed.

In the first instance, noise is introduced in the sense lines due to the air coupling between the sense lines and the drive lines. This component is proportional to $L \, di/dt$. Secondly, during reset time the $(2^n - 1)$ unselected cores are driven into saturation. This contributes an amount of noise which is proportional to $(2^n - 1) \frac{d\phi_k}{dt}$ where ϕ_k is the flux excursion between the remanent and saturation points of the core. This noise can be many times the output of the selected core.

The air flux coupling can be reduced by doubling back the sense line causing it to return at its starting point. This doubling back minimizes the area in which coupling can occur. The noise flux can be cancelled by providing sense line cancellation and/or by leaving the

inhibit lines on during the read phase as is suggested in Figure 4b, i.e., by using essentially DC. Noise line cancellation is provided in such a manner that one-half of the unselected cores threaded by a given sense line are threaded in a sense opposite to that which is given to the remaining half of the linked unselected cores. This will, in the worst case, leave one noise output uncanceled. Clearly, each sense line will have a unique cross-over point. Leaving the inhibit lines on during the read phase of the cycle does not interfere with the resetting of the selected core; it will, however, minimize the $d\phi_k/dt$ term. This mode of operation is defined as "damped". The outputs of a rope in the damped and undamped modes of operation are shown in Figure 6.

Rope Storage Elements and Speeds—Basically, two types of storage elements can be used in rope memories: bobbin cores and ferrites. The ferrites may be either square loop or linear. The advantage in using bobbin cores is that they require lower drives than ferrites, are relatively insensitive to large variations in the thermal environment, and give higher outputs per unit of area due to their higher flux density. Ferrites offer a wider opportunity for experimenting with different geometries and reducing parts of the manufacturing technique to a batch fabrication process⁹.

The ropes we have manufactured have been made with bobbin cores exclusively in order that they might meet required environmental specifications. It is possible to operate bobbin cores in a temperature range extending from -70°C to $+150^{\circ}\text{C}$. Using bobbin cores, we feel that the cycle times can at best be reduced to 6 μsec without resorting to overdriving. Using linear ferrites in novel geometries, cycle times of 2-4 μsec are attainable.

Rope Memory Applications

The function of data storage is common to all permanent memories. The data to be stored may typically consist of programs, constants, supervisory routines or abstracts; e.g., a capacitive memory developed by the Academy of Sciences of the USSR is used to store abstracts of scientific literature¹⁴. Rope memories are clearly capable of performing these functions.

The decision to use or not to use rope memories in these applications must then be based on such factors as cost, immunity to environment, speeds, selection techniques, and circuit requirements.

The rope has a built-in feature which is lacking in other types of permanent memories and which gives it a flexibility that extends its usefulness considerably. The rope is essentially a coding switch, and may thus be used to perform logic and lookup functions in a very efficient manner.

The use of ropes to perform logic (micro-programming) is straightforward and has been discussed by Walendziewicz in his paper on the Burroughs D210 Magnetic Computer²¹. In that computer, ropes are used both to perform logic and as fixed storage devices. The computer itself is used as a control element in various space and missile applications. Yii²³ has proposed and put into practice a scheme whereby every minterm in a Boolean function is represented by a core in a rope, and a wiring table is generated by negating the function and then applying De Morgan's Theorem. Using Yii's scheme, complements of the inputs are not always required.

The use of a rope memory as a dictionary in automatic language translation has been proposed⁸. If a source word is encoded in a standard six-bit code, the encoded source word will automatically select one core which can be made to store the target word. This overcomes the necessity for conducting a search. In this application, the D and C lines represent the encoded source word and its complement. If in addition to the target word, the complemented target word is also wired into the cores, the rope may serve as a two-way dictionary, e.g., Russian-English and English-Russian.

Rope memories can be used to effect information retrieval and association. For information retrieval purposes, a rope could operate in the one-core-per-word mode. The descriptors can be encoded in binary format. The binary coded descriptor then uniquely addresses a given core (or cores, in the case of multiple entries). Each core in turn stores the location of the required document. Content addressing can also be realized with rope memories by interchanging the

role of the sense and inhibit lines. The sense lines corresponding to bits used as the associative criteria are driven during the selection phase of the cycle. The particular combination of sense lines will cause all those cores storing information in accord with the search bits to be switched. During read time the addresses of all cores so switched can be determined by linking each core to a detector.

ROPE MEMORY MANUFACTURE

Rope memory manufacture is unique in that 1) no batch fabrication techniques are possible at the moment, 2) with the exception of the set, reset, and inhibit lines, there is no regular wiring pattern, 3) the test of the final assembly must establish that all cores are within specification at the end of the manufacturing process and that the information wired into the rope is correct.

Up to the moment, we have used only discrete cores as storage elements in rope memories. In the near future, we hope to be able to produce storage elements on a batch basis, using ferrites in conjunction with thick magnetic films⁹.

The main labor involved in the manufacture of a rope memory is in the wiring. This process has been automated to the fullest extent possible in order to reduce unit costs and to minimize the chances for human error. Rope memories are manufactured in modules of 256 or 512 cores. Initially, the set, reset, and inhibit lines are wired in. At this stage, the rope is tested to see that these lines were wired in correctly. This is done by driving each core in turn with a single turn winding and monitoring the output on the inhibit lines to determine whether or not a given inhibit line threads the core. After the rope passes this test, it is obvious that each core can be selected properly. The next step consists of wiring in the sense lines. For each sense line, there are as many thread, no-thread decisions as there are cores in the rope. All the thread, no-thread decisions for a sense line for 256 cores are encoded on a 90-column card. This card is used not only to govern the wiring phase of the manufacturing process, but also to test the correctness of the wiring. After each sense line is inserted, each core is addressed in turn and its output moni-

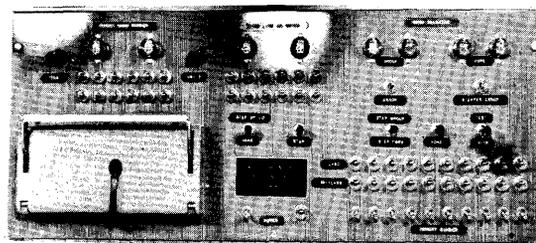


Figure 8. Sense line tester.

tored across that sense line. The output is compared to the information stored on the 90-column card. The sense line tester is shown in Figure 8. (The details of the manufacturing equipment and processes are the subject of a paper presently being prepared by the personnel responsible for its design.)

At the completion of the memory assembly, the rope is tested again. This final test consists of again testing each sense line as described above and/or reading out each word (core) in turn and comparing the wired word output against the desired word output, which is also stored on a 90-column card. Each rope is also tested to insure that the outputs of the whole assembly of cores are consistent with one another; i.e., that the cores meet their specification. This latter test is the third test that the cores are subjected to: they are first tested in a "raw" state to determine if they meet specifications, and they are again tested after mounting on the assembly matrix prior to being wired.

Packaging techniques are primarily dependent on the connector type used. Generally, ropes should be pluggable, which demands that a rugged connector be used. The choice of the connector is dependent on the size of the rope (256 or 512 cores) and the maximum number of sense lines. Our experience with packaging cores suggests that there are no difficulties in encapsulating a complete rope to protect it against environmental stresses.

ROPE MEMORY SYSTEM

As mentioned above, a number of rope memory systems have been built and placed into operation. A rope presently being designed and constructed is outlined in block diagram form in Figure 9. The purpose of this section is to

briefly outline the approach used in the design of this system.

The description of the rope memory system under construction is as follows:

STORAGE CAPACITY	256 words, expandable in modules of 256 words. Maximum number of bits per core: 64. Provision will be made for storing up to four words per core.
ADDRESS INPUT	Either serial or parallel. Only "true" address needs to be furnished. An eight-bit address input is required if one core stores one word. If cores store four words, a ten-bit address is required.
INFORMATION OUTPUT	Either serial or parallel.
STANDARD LEVELS	0 and -6 volts.
CYCLE TIME	8 μ sec.
POWER REQUIREMENTS	115 v AC, 60 cycles. Actual power will depend on memory configuration.
MECHANICAL	19" rack mount. Minimum height including power supply: 21". Rope memory will be interchangeable.
VERIFIER	A built-in verifier will allow each word to be addressed manually so that word content can be verified. Provision will be made for testing the memory under worst case drive conditions.

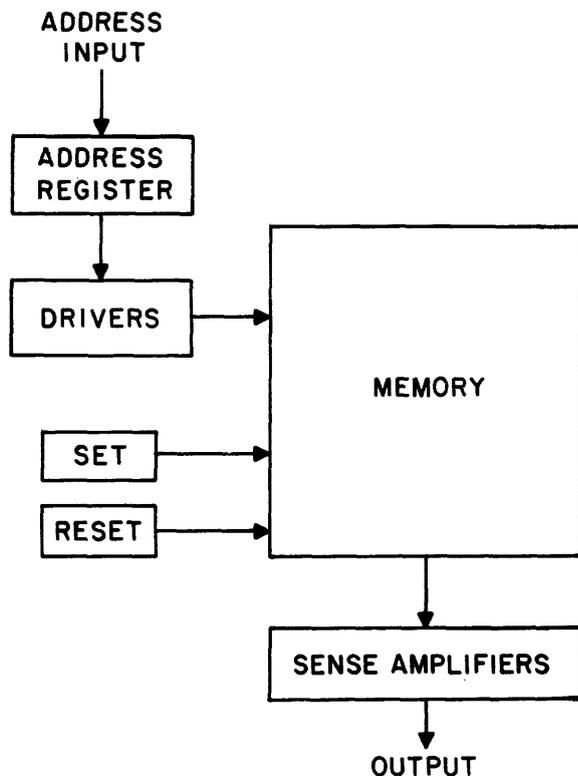


Figure 9. Rope memory system.

The eight-bit address of the core to be selected is the input to the rope memory system. The complement of the address is generated inter-

nally. If four 16-bit words are to be stored per core, giving a total storage capacity of 1024 words, the address must consist of ten bits: the eight low-order bits select the core, the remaining two bits are used to identify which of the four words stored by that core are to be read out.

Inspection of Figure 9 shows that no decoding circuits are necessary to select a core. All the information required for selection is contained in the address and its internally generated complement.

Selection may be accomplished in one of three different ways: 1) by having one driver associated with each of the direct and complemented address register bits and enabling those drivers whose corresponding bit position in the register is a "1"; 2) by using eight drivers and steering the current through the appropriate inhibit lines by means of switches controlled by the address register; 3) by using sixteen switches and activating eight of these to switch the proper inhibit lines from a zero level to a DC level able to generate the proper inhibit signal. The system under construction uses the last mentioned scheme. In addition, a set and reset driver are provided. The only restriction on the inhibit currents is that their amplitude be greater than that of the set pulse during the time the set pulse is turned on; no restrictions

are placed on the inhibit current waveforms. A damped mode of operation is used.

The output is fed into a flip-flop shift register. If four words are stored per core, the selected word will be gated to the output register by using the information contained in the additional two bits of the address.

The block diagram of a memory system utilizing an electromagnetic coupling type permanent memory³ is shown in Figure 10. The block diagram has been simplified for comparison purposes. A system of this type is inherently faster than a rope memory system since it depends on a coupling response proportional to di/dt and not on the switching time of a magnetic core. Since the output is dependent on di/dt , the rise time of the current pulse must be carefully controlled; in the rope system such careful control is not required as explained above. The input to that system is a nine-bit code. Six bits are used to select one of 64 channels. The remaining three bits are used to select one of eight words stored per channel—this corresponds to selecting one of four words stored per core in the rope memory system. There are 41 bits per word. The selection is accomplished by fragmenting the input as shown, and decoding each of the three segments

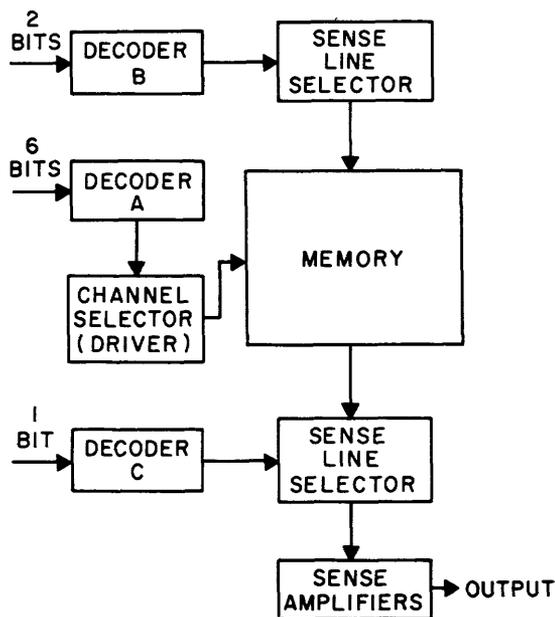


Figure 10. Electromagnetic coupling type permanent memory system.

in order to select the proper word. The address must be decoded as in any linear select scheme, a step not necessary in the rope memory system.

Due to the unique selection scheme employed by the rope memory and the fact that the tolerances on the inhibit drivers are very loose, together with the relative simplicity of the sense amplifiers due to the high output levels of the cores, the component count in such a system can be reduced by from 30% to 50% as compared to systems using other permanent memory schemes.

SUMMARY OF CHARACTERISTICS

A summary of various characteristics of the permanent memory schemes considered is given in Table III. Unfortunately, certain critical data is available only for the rope memory, and while it can be guessed what the comparable data is for other memory types, a comparison made on such a basis cannot be considered objective. For example, no data is available on the cost per bit of the various memory types discussed, nor is power consumption mentioned. In the rope memory, both cost per bit and power consumption are a function of core type used. Generally, as the flux is increased (for bobbin cores) both price and power consumption increase. Within limits, the cost per bit of a rope memory is the same as the cost per bit of a coincident current memory. Power requirements have been discussed above. Storage density in rope memories is between 500 and 800 bits per cubic inch.

The cycle times of all but the capacitive type memory appear capable of some improvement. As mentioned above, the use of linear ferrites as storage elements should make it possible to operate rope memories with a cycle time of 2-4 μsec . With regard to peripheral circuitry necessary to operate the various memories, the rope offers the greatest simplicity due to its unique selection scheme.

By adopting special packaging techniques, the addition of a limited number of data words is feasible in rope memories. Information can always be deleted by shorting out the unwanted core with a single-turn winding; up to ten new words can probably be put into a 256 core rope

TABLE III
SUMMARY OF CHARACTERISTICS

Permanent Memory Type	Changing Data Feasible?	Mechanical Alignment	Cycle Time	Output	Magnetic	Automatic Reset Required	Access	Bits Per Storage Element	Addressing
ROPE	NO	Not applicable	6-10 μ sec	100-200mv	Yes	Yes	Random	64+ depending on core	Null decoder
CAPACITATIVE	YES	Critical	200 μ sec	1mv	No	No	Random	1	Linear Select
EM COUPLING	YES	Critical	1 μ sec	50mv*	No	No	Random	1	Linear Select
PM TWISTOR	YES	Critical	5 μ sec	4mv	Yes	Yes	Random	1	Linear Select

* This value is computed and does not take attenuation into account.

to replace information deleted in this manner. While the other schemes allow wholesale alteration of information, the ease with which this can be done must be somewhat tempered by the mechanical alignment which is critical.

ACKNOWLEDGEMENTS

The work done with rope memories which forms much of the basis of this paper has depended on the cooperation of a number of people. It is with pleasure that I acknowledge the efforts of Messrs. W. Hennessey, A. Dorn, D. Pilsetnieks, and D. Clemson, all of the Electronic Instruments Division of the Burroughs Corporation. Messrs. Hennessey, Dorn and Pilsetnieks are responsible for the design of the rope memory manufacturing equipment and packaging techniques. Mr. Clemson is largely responsible for the realization of the test system, the coordination of the manufacturing procedure, and the work on the rope memory system described in the paper.

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